

region by introducing a first impurity into said impurity region through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

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introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 .

SUB 7
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7. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising:

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implanting an oxygen ion into a crystal semiconductor comprising a part to become a channel forming region by a convergent ion beam or an electron beam, said crystal semiconductor comprising silicon;

forming an intrinsic or substantially intrinsic region and an oxide region in said part to become the channel forming region by thermally treating said crystal semiconductor

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comprising silicon at a temperature of 1000 °C or higher to change a region of said crystal semiconductor implanted with said oxygen ion by said implanting step into said oxide; and introducing into said crystal semiconductor an impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween.

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9. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising:

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forming an intrinsic or substantially intrinsic region and an impurity region in a part of a crystal semiconductor to become a channel forming region by introducing a first impurity into said impurity region, said impurity region containing an element selected from the group consisting of carbon, nitrogen and oxygen as said first impurity; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said

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Concid direction of said channel width W, where $W_{pi}/W = 0.1$ to 0.9 and
 $W_{pa}/W = 0.1$ to 0.9 .

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D17 15. (Amended) A method of manufacturing an insulated gate
semiconductor device, said method comprising:

forming a resist over a crystal semiconductor comprising a
part to become a channel forming region;

forming a dotted hole in said resist by patterning said
resist using electron drawing method or FIB method;

C4 forming an intrinsic or substantially intrinsic region and
a plurality of impurity regions in said part to become the
channel forming region by introducing a first impurity into said
impurity regions through said resist having said dotted hole,
said first impurity being selected from the group consisting of
carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second
impurity that gives one conductivity to form a source region and
a drain region in said crystal semiconductor with said channel
forming region therebetween,

wherein said impurity regions form one or a plurality of
rows extending in a direction of a channel length of said
channel forming region, and

C4 Sub D'7
Concl'd wherein said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 .

20. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

C5 forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein an impurity element that expand an energy band width (E_g) is added to said impurity region, and

wherein said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 .

Sub 7
D1 23. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising:

forming a source region, a drain region and a channel forming region using a crystal semiconductor; and

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

C6 forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity region has an insulating property,

wherein an impurity element that expands an energy band width (E_g) is added to said impurity region, and

wherein said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 . --